REMARKS

Applicant thanks the Examiner for acknowledging the claim for priority under 35 U.S.C. § 119, and receipt of a certified copy of the priority document submitted July 6, 2001.

Applicant thanks the Examiner for considering the references cited with the Information Disclosure Statements filed July 6, 2001 and September 12, 2001.

Applicant thanks the Examiner for acknowledging the election without traverse of Group I, claims 1-16, in the Response to Restriction Requirement filed April 18, 2002.

Status of the Application

Claims 1-30 are all the claims pending in the Application, as claims 22-30 are hereby added to more fully describe the invention. Claims 1-8, 15 and 16 have been rejected. Claims 17-21 are withdrawn from consideration in view of the above election.

Allowable Subject Matter

Applicant thanks the Examiner for indicating that claims 15 and 16 would be allowed if rewritten to overcome the 35 U.S.C. § 112, 2nd paragraph rejections noted below.

Applicant thanks the Examiner for indicating that claims 9-14 would be allowed if rewritten in independent form.

Drawing Objections

The Examiner has objected to the drawings for informalities. The informalities noted by the Examiner have been corrected in the Proposed Drawing Corrections submitted herewith. Thus, withdrawal of the drawing objections are respectfully requested

Indefiniteness Rejection of Claims 4-7, 15 and 16 Under 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected claims 4-7, 15 and 16 as being indefinite under 35 U.S.C. § 112, second paragraph.

With respect to claims 4 and 7, the Examiner has taken the position that the recited "bypass capacitor" (in claim 4) and the "input/output device" (in claim 7) lack antecedent basis because these features were "only earlier defined as one element of a Markush group in claim 2."

However, Applicants respectfully submit that claim 2 does not recite a Markush group, in contrast, claim 2 recites that the device can be comprised of one or more of the recited features. Applicants respectfully submit that such alternative claim language is specifically allowed by *MPEP § 2173.05(h)(III)*, and that claim 2 therefore provides correct antecedent basis for the "bypass capacitor" and "input/output device."

Thus, Applicants respectfully request the Examiner to withdraw the rejections of claims 4-7.

Regarding claims 15 and 16, the informalities noted by the Examiner have been corrected. Thus, withdrawal of the claim rejections are respectfully requested.

Anticipation Rejections of Claims 1, 2, 4-6 and 8 Under 35 U.S.C. § 102(b)

The Examiner has rejected claims 1, 2, 4-6 and 8 under 35 U.S.C. § 102(b) as being anticipated by Mori (US 5,949,098; hereinafter "Mori"). This rejection is respectfully traversed.

Claim 1

The Examiner has taken the position that Mori discloses, in FIGS. 3 and 4, "a semiconductor device having ... an inner area 421/422 at a surface and a pad area (generally the

area including pads 433) surrounding the inner area therein, the semiconductor device comprising a device fabricated below the pad area (see figure 3)."

In contrast to the Examiner's assertion, Mori is directed towards "an improved arrangement of power supply lines" (col. 1, line 13). Specifically, FIG. 3 of Mori cited by the Examiner is not a section through the pad area at all. Rather, FIG. 3 is a vertical cross-sectional view of the third embodiment of Mori, showing the structure below power wiring layer 310, which forms power conducting line 311. There is no teaching or suggestion that the power conducting line 311 is located in the pad area of any semiconductor device disclosed in Mori.

In fact, the embodiments disclosed in FIGS. 4 and 5 of Mori show a chip layout that "is configured using the power/ground conductive line employed in any one of the first through third embodiments" (col. 5, lines 57-60; col. 6, lines 25-29). These FIGS. show "power/ground conductive line 411 provided in a ring form inside a power pad 431, a ground pad 432, and input/output pads 433" (col. 5, lines 64-66), and a "power/ground conductive line 511 disposed entirely inside a power pad 531, a ground pad 532 and input/output pads 533" (col. 6, lines 33-36).

Thus, Mori discloses that the power conducting lines 111, 211 and 311 are actually provided inside of any portion that could be considered to be the pad area of Mori, and therefore cannot teach or suggest "a device fabricated below said pad area," as recited in claim 1. There is no teaching or suggestion that the features shown in FIGS. 1-3 extend anywhere else besides directly under the power conducting lines themselves.

Thus, for at least the above reasons, Applicants respectfully request that the Examiner withdraw this rejection.

Claims 2, 4-6

Claims 2, 4-6 are dependent, directly or indirectly, from claim 1, and therefore Applicants respectfully submit that these claims are allowable, at least by virtue of this dependency.

Claim 8

The Examiner has taken the position that Mori discloses all the features of claim 8 (see page 4 of the Office Action). Specifically, the Examiner proffers that Mori discloses "a first source voltage wire (e.g. 310) connected to a source voltage Vdd and surrounding the innner area in the pad area and a first ground wire (e.g. 350) being grounded and surrounding the first source voltage wire in the pad area."

However, Applicants respectfully submit that Mori does not teach or suggest either a first source voltage wire, or a first ground wire "in said pad area," as recited in claim 8. As discussed in detail above, the portions (310, 350) cited by the Examiner as the claimed wires are located inside of any portion that could be considered to be the pad area of Mori.

Additionally, Applicants respectfully submit that Mori does not teach or suggest that a first ground wire surrounds a first source voltage wire. In contrast to the Examiner's position, FIG. 3 shows power wiring layer 310 above ground wiring layer 350, in a vertical cross section

of a semiconductor device. Thus, FIG. 3 discloses that the cited wiring layers are actually in the same vertical plane, and thus neither can be read as surrounding the other.

Thus, for at least the above reasons, Applicants respectfully request that the Examiner withdraw this rejection.

Anticipation Rejections of Claims 1-5 Under 35 U.S.C. § 102(b)

The Examiner has rejected claims 1-5 under 35 U.S.C. § 102(b) as being anticipated by Sudo (JP 5-55380; hereinafter "Sudo"). This rejection is respectfully traversed.

Claim 1

Sudo is discussed in detail in the instant Application, on page 3, lines 2-7.

The Examiner has taken the position that Sudo discloses "an inner area 11 at a surface and a pad area 1 surrounding the inner area therein, the semiconductor device comprising a device fabricated below the pad area (see fig. 1b)."

In contrast to the Examiner's assertion, it is clear that the elements shown in FIG. 1b of Sudo are located below power wiring layer 9 and grounding wire layer 11, and that power wiring layer 9 and grounding wire layer 11 are located entirely within any portion of substrate 1 that could be considered to be the "pad area" recited in claim 1 (see FIG. 1a). Thus, the detail of FIG. 1(b) cannot teach or suggest "a device fabricated below said pad area," as recited in claim 1.

Additionally, the embodiments shown in FIGS. 2-4 are similarly lacking in any disclosure of devices under the pad layer, as claimed. FIG. 2(b) only show detail below power

wiring layer 209 and grounding wiring layer 211, and FIG. 3(b) only shows detail below power wiring layer 303 and grounding wire layer 304. There is simply no teaching or suggestion that such detail extends anywhere below the pad areas disclosed in these FIGS. Thus, none of these embodiments can teach or suggest "a device fabricated below said pad area," as recited in claim 1.

Claims 2-5

Applicants respectfully submit that all claims 2-7 that are dependent from claim 1 are allowable, at least by virtue of that dependency.

Obviousness Rejections of Claim 7 Under 35 U.S.C. § 103(a)

The Examiner has rejected claim 7 under 35 U.S.C. § 103(a) as being unpatentable over Mori in view of Applicants' Admitted Prior Art (hereinafter "AAPA"). This rejection is respectfully traversed.

Applicants respectfully submit that claim 7 is allowable, at least by virtue of its dependency.

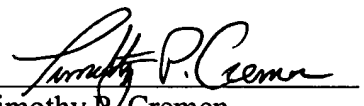
Conclusion

In view of the foregoing, it is respectfully submitted that claims 1-30 are allowable. Thus, it is respectfully submitted that the application now is in condition for allowance with all of the claims 1-30.

If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Please charge any fees which may be required to maintain the pendency of this application, except for the Issue Fee, to our Deposit Account No. 19-4880.

Respectfully submitted,



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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification is changed as follows:

The third full paragraph on page 16 is amended as follows:

The VDD wire 26a has the same structure as that of the VDD wire [26b] 16b, and the GND wire 27a has the same structure as that of the VDD wire [27b] 17b. A positional relationship between the VDD wire 26a and the GND wire 27a is identical to the positional relationship between the VDD wire [26b] 16b and the GND wire [27b] 17b.

The fourth full paragraph on page 16 is amended as follows:

As illustrated in Fig. [7B] 7C, the VDD wire 26b formed in the pad area 13 is electrically connected to the VDD wire 26a formed in the input/output area 12 through a first electrical connector 28. Similarly, as illustrated in Fig. [7C] 7B, the GND wire 27b formed in the pad area 13 is electrically connected to the GND wire 27a formed in the input/output area 12 through a second electrical connector 29.

The paragraph bridging pages 16 and 17 is amended as follows:

In accordance with the second embodiment, the bypass capacitor could have an increased capacity, because an additional capacity is defined [between the teeth of the VDD wire 26a and teeth of the GND wire 27a, and further] between the teeth of the VDD wire 26b and teeth of the GND wire 27b.

The fifth full paragraph on page 17 is amended as follows:

The protection device [13] 31 is comprised of a substrate 20 formed at a surface with a n-type well 32a and a p-type well 32b, a first interlayer insulating film 20a formed on the substrate 20, a first layer 20b formed on the first interlayer insulating film 20a, a second interlayer insulating film 20c formed on the first layer 20b, and a second signal wiring layer 33 formed on the second interlayer insulating film 20c.

IN THE CLAIMS:

The claims are amended as follows:

15. (Amended) A semiconductor device having a plurality of wiring layers in a multi-layered structure,

said semiconductor device including an inner area at a surface, an input/output area surrounding said inner area therein, and a pad area surrounding said input/output area therein,

said semiconductor device including a plurality of input/output terminals in said input/output area, and a plurality of pads in said pad area,

said semiconductor device including (a) a first source voltage wire being electrically connected to a voltage source and surrounding said inner area in said pad area, and (b) a first ground wire being grounded and surrounding said first source voltage wire in said pad area,

each of said pads being electrically connected to any one of said input/output terminals, said first source voltage wire, and said first ground wire,

said semiconductor device including a protection device fabricated below said pad area,

said protection device comprising:

(a) a substrate formed at a surface with a first well having a first electrical conductivity and a second well having a second electrical conductivity;

(b) a first interlayer insulating film formed on said substrate;

(c) a first layer formed on said first interlayer insulating film;

(d) a second interlayer insulating film formed on said first layer; and

(e) a signal wiring layer formed on second interlayer insulating film,

said first layer including [one of said] a first metal wiring [layers, one of said] layer, a second metal wiring [layers] layer, and a second signal wiring layer all electrically connected to said first or second well through via-holes formed through said first interlayer insulating film,

said second signal wiring layer being electrically connected to said signal wiring layer through via-holes formed through said second interlayer insulating film.

16. (Amended) A semiconductor device having a plurality of wiring layers in a multi-layered structure,

said semiconductor device including an inner area at a surface, an input/output area surrounding said inner area therein, and a pad area surrounding said input/output area therein,

said semiconductor device including a plurality of input/output terminals in said input/output area, and a plurality of pads in said pad area,

said semiconductor device including (a) a first source voltage wire being electrically connected to a voltage source and surrounding said inner area in said pad area, and (b) a first ground wire being grounded and surrounding said first source voltage wire in said pad area,

each of said pads being electrically connected to any one of said input/output terminals, said first source voltage wire, and said first ground wire,

said input/output area having an extended portion located below said pad area,

said extended portion comprising:

(a) a substrate formed at a surface with a first well having a first electrical conductivity and a second well having a second electrical conductivity;

(b) a first interlayer insulating film formed on said substrate;

(c) a first layer formed on said first interlayer insulating film;

(d) a second interlayer insulating film formed on said first layer; and

(e) a signal wiring layer formed on second interlayer insulating film,

said first layer including [one of said] a first metal wiring [layers] layer electrically connected to said first well through a via-hole formed through said first interlayer insulating film, [one of said] a second metal wiring [layers] layer electrically connected to said second well through a via-hole formed through said first interlayer insulating film, and a second signal wiring layer electrically connected to said first or second well through via-holes formed through said first interlayer insulating film,

said second signal wiring layer being electrically connected to said signal wiring layer through via-holes formed through said second interlayer insulating film.

Claims 22-30 are added.